Analog Design Challenges in Advanced CMOS Process Node

Dejan Mirković, Predrag Petković and Dragiša Milovanović

Abstract – This paper deals with problems of porting integrated circuit (IC) designs to new, scaled, process node. A problem arises especially when analog part of the chip has to be transferred. New process nodes provide many high end capabilities e.g. high speed and low power consumption. On the other more and more parasitic and higher order effects comes in to play. Therefore, extensive simulations of standard MOS device are obligated in order to unveil true device behaviour which is crucial in the world of analog IC design. For the characterization purposes Cadence® Open Command Environment for Analysis (OCEAN) in conjunction with GNU Octave is exploited. Conclusions regarding design strategies are extracted. Important trade-offs are to be pointed out, as well.

Keywords – CMOS Process nodes, analog integrated circuits, simulation, MOS device

I. Introduction

Contemporary submicron processes are primarily focused on improving device characteristics in digital domain. Main motive behind aggressive dimensions and power supply voltage shrinking lies in possibility to obtain higher operation frequency and lower power consumption. Practically, as far as digital circuitry is concerned the most important operation is to efficiently (as fast as possible and with smallest amount of energy burned) turn off and on MOS device (switch). Highest frequency at which single device can operate is defined as unity current gain frequency, f_T, i.e. when drain and gate current ratio, i_d/i_g, equals one. This frequency can be easily estimated if one consider common source topology with dominant gate terminal parasitic capacitance, $C_{GG} = C_{GS} + C_{DS}$ (which for long channel device becomes $C_{GG} \approx C_{GS}$). Since drain current is g_m times V_{GS} and V_{GS} lies across C_{GS} relation between i_d and i_g arises. In saturation (strong inversion) C_{GS} can be further approximated with $2C_{ox}W/3$ where C_{ox} is gate oxide capacitance density. For square low devices g_m equals $\mu C_{ox}W(V_{gs} - V_{th})/L$, where $V_{gs} - V_{th}$ is overdrive voltage, V_{ov}, and μ, W and L stands for carrier mobility, width and length of the MOS device, respectively. Finally, approximated f_T expression for long channel device is given in (1).

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$$f_T = \frac{g_m}{2\pi C_{GG}} \propto \frac{3\mu V_{ov}}{4\pi L^2} \qquad (1)$$

From (1) it is obvious that shorter devices with larger overdrive voltage will operate at higher frequency.

It is already known that dominant load in CMOS technology has capacitive character and that the maximum power consumption occurs when charging/discharging that capacitive load, C_{load}. Maximum switching current, $I_{D\max}$, can be related with switching frequency, f_{sw}, and worst case voltage change across capacitive load, $\Delta V_{D\max}$, as given in (2).

$$P_{sw} = I_{D\max}\Delta V_{D\max} \propto 2\pi f_{sw} C_{load} V_{DD}^2 . \qquad (2)$$

Worst case voltage change corresponds to entire power supply swing from 0V to V_{DD}. Therefore, (2) unveils motive to keep power supply as low as possible in order to reduce dynamic power consumption.

All these properties, towards deep submicron process nodes strive, only help digital operation. Analog IC circuitry often has exactly the opposite requirements. Sometimes one needs to sacrifice power consumption to fulfil noise and speed constraints like in mixed-signal circuits. In other cases such as low power RF applications week inversion region is used in order to accomplish high speeds and keep low power consumption. Practically there is always a trade off between several quantities (power, speed, delay, noise, signal swing etc.). Power supply and dimension shrinking in submicron processes only makes things worse and puts additional design challenge for analog IC design. As a result effects like leakage mechanisms (reverse biased junction current, gate induced drain leakage, direct gate tunnelling, sub-threshold leakage) which boosts up static power consumption and drain induced barrier lowering, lower gate-oxide breakdown voltage etc. arises [1], [2], [3]. Aside of these effects, V_{th} do not scale linearly with V_{DD} [4]. This phenomenon of drastic voltage headroom reduction causes the main anlaog design challenge.

Prime goal of this paper is to provide overview of deep submicron, 65nm, process and emphasize differences comparing to 350nm process. Besides, 65nm nod will be the target technology for the new Integrated Power Meter (IMPEGIII) chip developed in LEDA laboratory [5]. Deep submicron 65nm is compared with 350nm process from standpoint of MOS deice capabilities. Even it is considered obsolete and replaced with younger, 180nm and 90nm nodes; it is still favourable for analog and mixed-signal design. Previous version of IMPEG chip was implemented in 350nm technology hence the reason for choosing it for comparison.

In the following section some guidelines about important device characteristics and how to obtain them will be given. Environment used to automate simulation process will be disused. Then, in the third section, 350nm and 65nm process nodes MOS device will be compared through simulation results. Conclusion will summarise important findings obtained from previous sections.

II. Device Characteristics

This section will cover major device characteristics and provide insight to appropriate test bench circuits used to extract them. More detailed information covering device models, results from exhaustive corner analyses and measurements of a single device are contained in proprietary Process Design Kit (PDK) documentation. However this documentation does not provide relation between key design parameters (e.g. gain, bandwidth) and device dimensions. Therefore it is necessary to examine device behaviour when applied in real circuit environment (e.g. with feedback). For sake of simplicity all further discussed circuits are for the NMOS device and can easily be adjusted to apply on PMOS.

A. Intrinsic small signal gain

Maybe the most important design parameter of the analog circuit is its small signal voltage gain. When a new process node shows up in the market designers are usually interested in “how much gain the smallest device can provide”. Using the small signal model of the MOS FET (3) is obtained:

$$A_{v0} = g_m r_0 = \frac{2V_E L}{V_{ov}}, \tag{3}$$

where g_m and r_o are small signal parameters, transconductance ($2I_D/V_{ov}$) and resistance ($V_E L/I_D$), respectively. Here I_D stands for transistor bias current and V_E represents process dependent parameter expressed in volts over meters [6]. This process parameter can be thought of as equivalent for the Early voltage of bipolar transistor. From (3) it is obvious that the increasing device length increases gain, at least at DC. Since V_E parameter depends strongly on process it cannot be accurately estimated. Therefore the simulation is standard way for small signal gain extraction. For this purpose test bench circuit in Fig. 1 is used.

This circuit simulates real working environment of the device. DC current through device is always determined by some external bias circuit and mirrored to I_{bias}. This current sets appropriate V_{ov} and consequently V_{GS}. In order to keep device in linear region and at the same time sweep DC voltage across it positive feedback is established through an ideal opamp. This way V_{DS} is forced to track V_{ref} change while preserving bias point set by I_{bias}. The whole structure practically behaves similarly to diode connected device with fixed bias current.

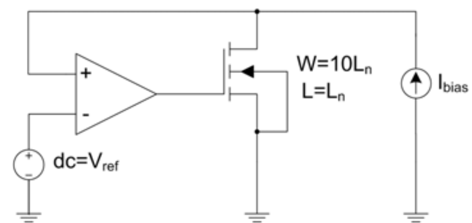


Fig. 1 Test bench circuit for A_{v0} simulation

Circuit in Fig. 1 is proved to be quite popular test bench since it requires smallest number of sweep parameters.

Two test cases are preformed. First V_{ref} is swept with I_{bias} fixed in order to examine A_{v0} versus V_{ov}. In the second case I_{bias} is swept while V_{ref} remains constant. Sweep simulations are repeated for different L_n values. These tests extract A_{v0} behaviour for different device lengths and bias conditions.

B. Composite figure of merit

Besides small signal gain, equally important device parameter is the unity current gain frequency, f_T. It determines how fast device can operate at given bias point.

Since voltage headroom is drastically reduced in deep submicron processes it is inevitable that some devices will be forced to operate at the edges of the strong-weak inversion region. Not infrequently happens that only sub threshold reign is used [7]. Therefore drain current square low dependence is no more valid. This implies that hand calculations are irrational to use when designing device in submicron process nodes. The common method for mapping design parameters to transistor bias points and consequently dimensions is g_m/I_D curve. This ratio is often called device efficiency because it tells how much transconductance per bias current can be obtained. Using this measure one can ensure not to spend too much current (energy) for required transconductance. Therefore power efficient design is ensured.

In order to find optimal bias point of the device so called Composite figure of merit (CFOM) should be extracted. Expression for CFOM is $f_T \times g_m/I_D$ and its maximum gives optimum bias point.

For extraction of all these parameters diode connected device is used. Fig. 2 illustrates test bench circuit. Here sweep parameter is V_d. Since V_{DS} equals V_{GS} saturation is ensured. Again sweep simulation is repeated for different channel lengths.

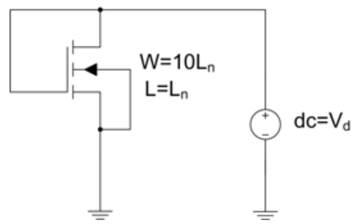


Fig. 2 Test bench circuit for CFOM simulation

C. Noise

Next aspect of importance is the noise. Reduced supply voltage implies smaller signal swings. As the signal amplitude become smaller the noise influence increases. Test bench circuit is shown in Fig. 3.

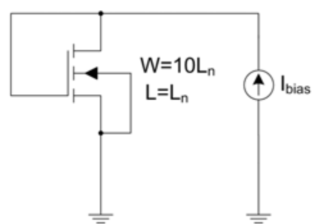


Fig. 3 Test bench circuit for noise performance simulation

Again diode connected device is exploited but with fixed DC current. Since ideal current source ensures infinite load impedance only device noise influence is present. Noise analysis is performed for different device lengths.

For simulation Cadence® Spectre simulator is used. Since a number of parametric sweep simulations are required the procedure is automated using SKILL scripting language in OCEAN under Cadence Design System® (CDS) [8]. This way call of a single script performs all necessary simulations. Even CDS contains plotting programs usually they do not provide enough degree of freedom and control over plotting process. Therefore GNU Octave is used for data presentation. GNU Octave is an open-source alternative to MATALB®, proprietary programming framework for numerical mathematics and data analysis [9]. Both platforms provide a large number of useful mathematic operations and functions, support interactive and batch mode, and run under UNIX/Linux operating systems. All this makes them compatible and attractive to be combined into one unit.

The subsequent section will present results obtained using described software conjunction for simulation of aforementioned test benches. The procedure will be implemented on two process nodes.

III. Simulation Results

As announced in Section I transistor performances of two process nodes will be compared. Transistors are from the same, Taiwan Semiconductor Manufacturing Company (TSMC), manufacturer. Both types i.e. NMOS and PMOS devices are examined. Since both showed the similar differences in terms of A_{v0}, f_T, g_m/I_D and CFOM in two different processes only results for NMOS are presented. Exception is comparison from noise performance point of view. For this case both device types are presented. Three channel lengths are chosen as shown in Table I.

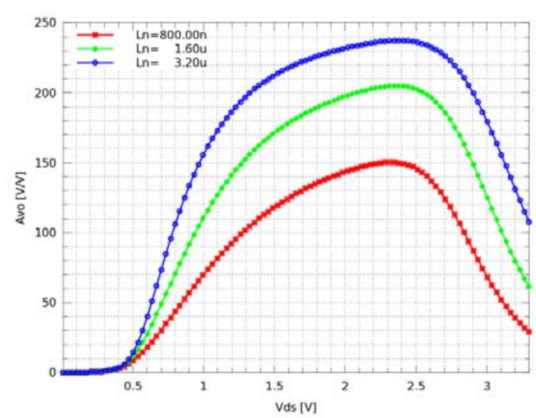
TABLE I
DEVICE LENGTHS

Process	Length [µm]		
350nm	0.8	1.6	3.2
65nm	0.24	0.48	0.96

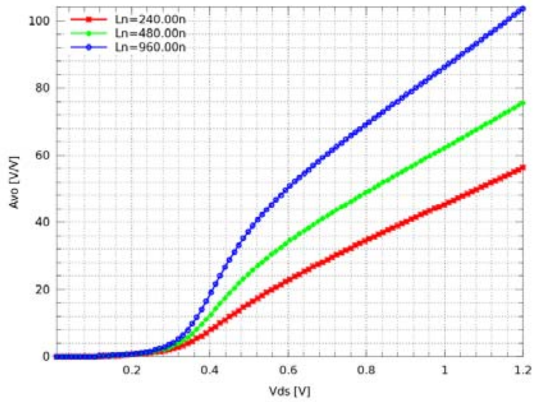
To minimise small channel effect twice the minimal for 350nm and three times the minimal for 65nm process length is adopted as a start value for device length. For all cases device width is chosen to be ten times the length. These are the common proportions for the smallest device in analog IC application.

Firstly, small signal voltage DC gain is examined. Fig. 4 shows this parameter versus output voltage, V_{DS}, for 250 µA fixed bias current, I_{bias}.

It is important to mention that this is a purely DC measure and therefore such large values for the gain. First thing to notice from Fig. 4 is different power supply arrangement, 3.3V for 350nm vs. 1.2V for 65nm. E.g. V_{DS} bias of 1.2V and two times the minimal transistor length, 800nm, provides a gain of about 100 in 350nm process. This is obtained for bias of about a third of the V_{DD}. To achieve the same gain in 65nm process one needs to use nearly a full power supply i.e. 1.2V and at least 16 times larger length than minimal, 960nm.



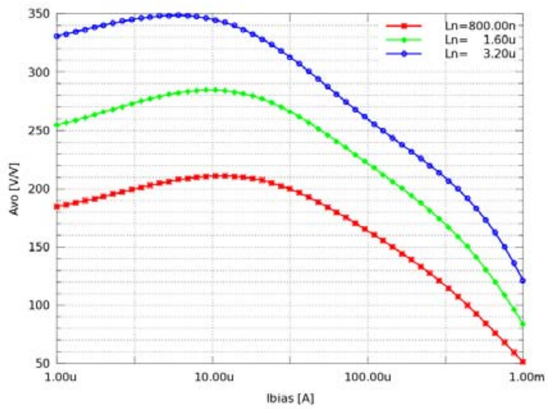
a) For 350nm



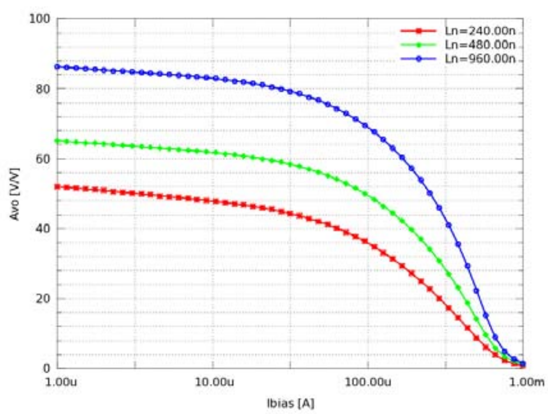
b) For 65nm

Fig. 4 Small signal DC gain vs. drain source voltage

Fig. 5 presents the small signal DC gain versus different bias currents and fixed reference voltage, V_{ref}, of $V_{DD}/2$.



a) For 350nm



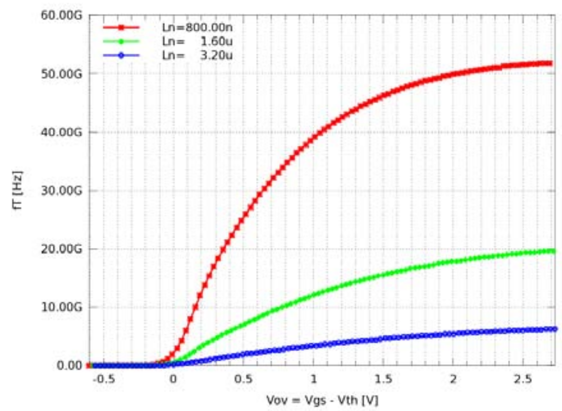
b) For 65nm

Fig. 5 Small signal DC gain vs. drain bias current

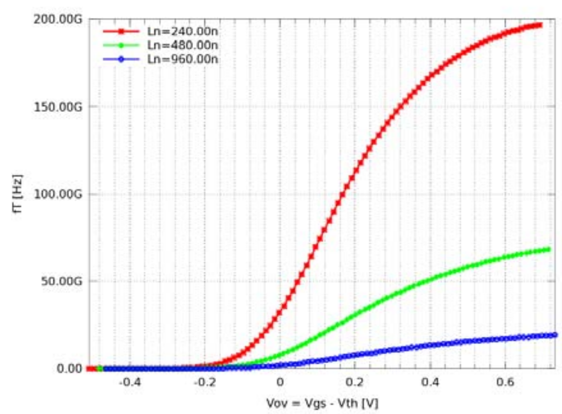
It is obvious that increasing bias current does not solves the gain reduction in sub micron process nodes. Therefore, besides standard cascoding, advanced design techniques such as gain boosting, bootstrapping and current cancelation should be used [6].

Unfortunately threshold voltage V_{th} also changes with transistor dimensions. For these test cases simulation results showed that V_{th} ranges from 0.57÷0.61V for 350nm and 0.47÷ 0.51V for 65nm process. This results in absolute, ΔV_{th}, change of 40mV. V_{th} fluctuation in sub micron process becomes influent because of reduced voltage headroom. That is why it is not wise to use it as reliable design parameter.

Fig. 6 shows f_T dependence on overdrive voltage. It is clear that new sub micron processes provide higher speed for nearly an order of magnitude. Certainly, this is only valid for small device lengths. Increasing length for the same bias conditions reduces operating frequency as (1) suggests.



a) For 350nm



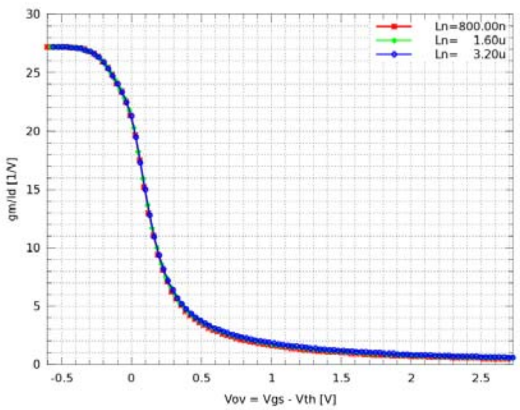
b) For 65nm

Fig. 6 Unity current gain frequency vs. overflow voltage

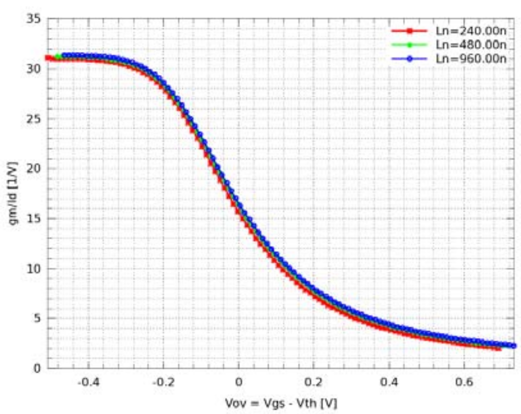
On the other choosing larger V_{ov} increases f_T. This fact should be used with caution because larger V_{ov} reduces device efficiency as shown in Fig. 7.

Fig. 7 shows that device efficiency is the only reliable design parameter i.e. it is relatively independent on device dimensions and other effects (short channel, carrier velocity saturation etc.). Shape of the curve is the same for both process nodes. Value of g_m/I_D at sub threshold edge, $V_{ov} = 0$V, is 15 for 65nm and it is lower comparing to 20 for 350nm. But submicron node provides higher efficiency in week inversion region then 350nm node, 32 versus 27. Hence reason to exploit this region of operation in sub micron processes.

The best way to establish optimal V_{ov} is to look at CFOM. This parameter is presented in Fig. 8.



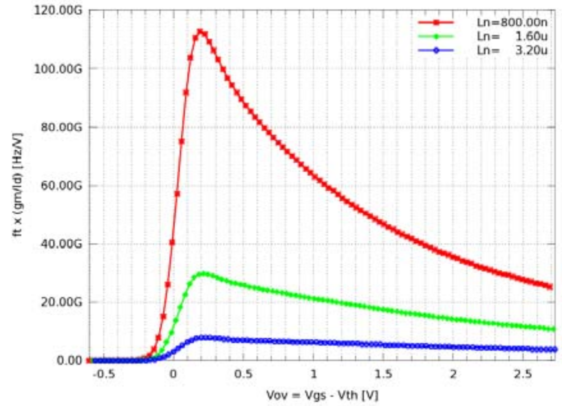
a) For 350nm



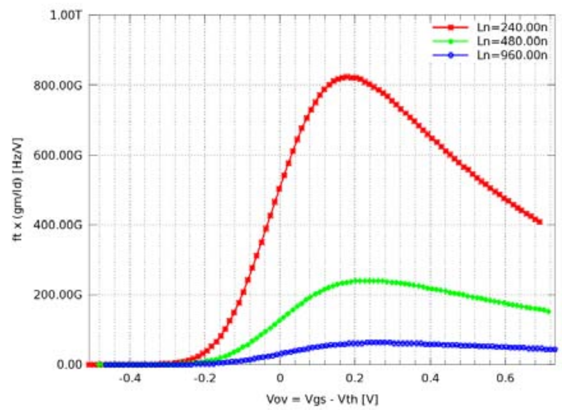
b) For 65nm

Fig. 7 Efficiency vs. overflow voltage

CFOM has its maximum for about 0.2V of overdrive voltage for both process nodes. It is important to notice that this value did not scale down with V_{DD} at all. Let us assume that one half of the V_{DD} dedicates to signal range and the other half to transistor bias. Older, 350nm node, will allow about eight devices in the cascode while newer, 65nm node, only three. Therefore, sub threshold region of operation and consequently advanced design techniques are inevitable in submicron process nodes especially when low power is required.



a) For 350nm

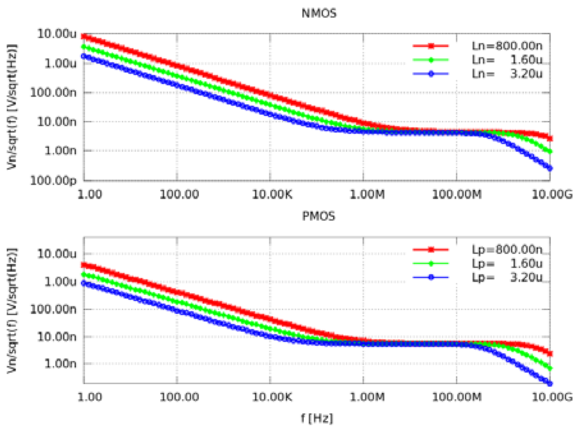


b) For 65nm

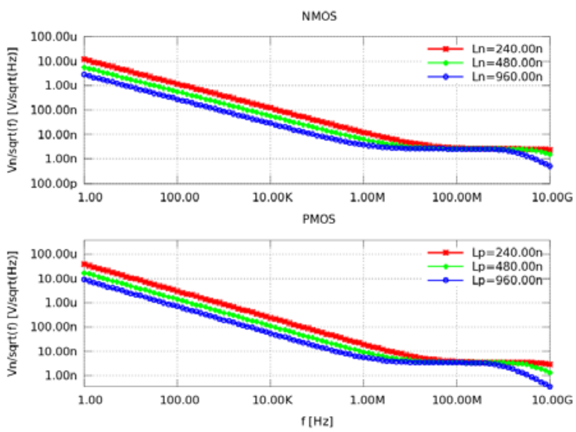
Fig. 8 Unity current gain frequency, Efficiency product vs. overdrive voltage

Finally noise performance is presented in Fig. 9. Here comparison between NMOS and PMOS devices is given. Bias current is fixed at 250 μA. In both types of device same $W/L = 10$ is used. For 350nm nod NMOS device has a larger flicker noise and corner frequency then PMOS device. This is quite expected since both NMOS and PMOS devices uses N type polysilicon gate. This prevents forming the channel at the surface directly under the gate oxide in PMOS devices. Practically PMOS devices have buried channel with smaller possibility of random trapping/releasing carriers at the oxide/channel surface. This mechanism is known as the main source of flicker noise in MOS devices [10].

However 65nm node exhibits opposite behaviour. Actually NMOS device shows better performance then PMOS device. This is because both types of the device have surface channels. This means that PMOS uses P type and NMOS uses N type polysislicon gate. Therefore there is no advantage in favour of PMOS over NMOS. However this is very technology dependent property hence important to examine. Table II summarises total noise contribution for both process nodes.



a) For 350nm



b) For 65nm

Fig. 9 Noise performance

TABLE II
TOTAL NOISE CONTRIBUTION

Frequency range 1Hz ÷ 10GHz		Integrated noise power [V^2]			
		NMOS		PMOS	
		1/f	thermal	1/f	thermal
Length for 350nm [µm]	0.8	1.46n	0.14µ	0.37n	0.16µ
	1.6	0.29n	56.2n	73.1p	58.1n
	3.2	62.8p	16.4n	15.5p	16.3n
Length for 65nm [nm]	240	3.23n	59.9n	13.2n	0.106µ
	480	0.73n	44.8n	2.74n	58.8n
	960	0.16n	17.2n	0.68n	17.6n

Again, looking at results in Table II, PMOS provides better noise performance than NMOS in 350nm and vice versa in 65nm process nod.

IV. CONCLUSION

This paper examined problems and challenges concerning analog IC design. General conclusion is that sub threshold region of operation and advanced design techniques are almost obligated in sub micron process nodes. It was also shown that some previously acquired rules of thumb from older process nodes such as one concerning noise performance are no more valid. Therefore it is of crucial importance to examine device behaviour before considering to port design to new process nod. It is clear that at least analog part of the design has to be designed nearly from scratch.

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REFERENCES

[1] Roy, K., Mukhopadhyay, S., Mahmoodi-Meimand, H., *"Leakage Current Mechanisms and Leakage Reduction Techiques in Deep-submicrometer CMOS circuits"*, Proceedings of the IEEE, Vol. 91, No. 2, Feb., 2003, pp. 305-327.

[2] Jovanović, B., Damnjanović, M., *"Low Power Techniques for Leakage Power Minimization"*, Proceedings of LIV ETRAN Conference, Jun., 2010., pp. EL3.4-1-4.

[3] Borkar S.,*"Design Challenges of Technology Scaling "*, IEEE Micro, Vol. 19, No. 4, Avg., 1999, pp. 10-16.

[4] Gonzalez, B., Gordon, M., *"Supply and threshold voltage scaling for low power CMOS"*, IEEE Journal of Solid State Circuits, Vol. 32, Issue 8, Aug., 1997, pp. 1210-1216.

[5] Litovski, V., et al., *"IMPEG 2"*, Technical Solution – laboratory prototype TR 6108B, Apr., 2008.

[6] Sansen, W., “*Analog Design Essentials*”, Springer, Dordrecht, Netherlands, 2006.

[7] Dokić, B., Pajkanović, A., *"Low Power CMOS Sub-Threshold Circuits"*, Int. Simp. µPRO2013, May, 2013.

[8] “*OCEAN Reference*”, Cadence Design Systems, Inc., San Jose, 2004.

[9] http://en.wikipedia.org/wiki/GNU_Octave, 2013.

[10] Reimbold, G., *"Modified 1/f Trapping Noise Theory and Experiments in MOS transistors Biased from Weak to Strong Inversion – Influence of interface states"*, IEEE Transaction on Electron Device, Vol. ED-31, No. 9, Sep., 1984, pp. 1190-1198.